Name	:	Dr. Manoj Saxena
Designation	:	Senior Lecturer, Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi,
Postal address for Communication	:	Dr. Manoj Saxena, Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi, Karampura, New Delhi-110015
Phone Number(s)	:	Office : 011-25458173 Residence : 011-28531418 Mobile : 09968393104
Fax Number(s)	:	Not Available
E-mail address	:	saxena_manoj77@yahoo.co.in, saxenamanoj77@gmail.com, msaxena@ddu.du.ac.in,

Brief account of research interests with special focus on Nano Science and Technology (strictly within 300 words):

I have been working for more than Seven years in the area of Micro/Nanoelectronic device modeling and simulation with significant device design innovations in the area of: Novel Gate Electrode Workfunction Engineered MOSFET, insulated shallow extension (ISE) MOSFET and Silicon On Nothing MOSFET and has authored or coauthored 81 technical papers in International journals and various conferences.

In 2002, we reported perhaps for the first time a two-dimensional analytical model for Si-Bulk Dual Material gate MOSFET (DMG-MOSFET) which ensures screening of drain potential variation by the gate near the drain, which in turn improves the carrier transport efficiency. Later, five new nanoscale MOSFET designs were proposed: DUMGAS, ASYMGAS, DMGASYMOX and TRIMGAS and HEM-DG. Later, using a unified analytical threshold voltage model can, electrical characteristics of 16 different Sub-120 nm MOSFETs were analyzed. In 2007, a compact model for Non Uniformly Doped Channel (NUDC) MOSFET was reported, that can model almost all type of channel engineered structures such as Epi-layer, Graded channel (GC), Lightly doped drain (LDD), Halo, Pocket implant technology etc. The model incorporates DIBL effect using Voltage Doping Transformation (VDT) method, which replaces the influence of the lateral drain-source field by an equivalent reduction in the channel doping concentration. Substantial theoretical contributions, were made by developing compact models for Sub-50 nm nanoscale ISE MOSFET for mixed mode applications and hot carrier reliability using extensive simulation studies for studying non-local transport mechanisms due to electronic temperature gradients. Recently, we optimized 40 nm gate length nanoscale DMG-SON MOSFET with 41dB open-loop voltage gain in cmparison to 17dB for that of SMG SON MOSFET.Superior transconductance generation efficiency, low output conductance properties and better f_T – gain

relationship of DMG configuration when supplemented with gate stack configuration further increases the intrinsic gain upto 54dB.

Keywords related to your research interests (maximum 10, different lines separated by commas)

Semiconductor device modeling and simulation,
non-classical nanoscale MOSFET architectures,
grooved/trench gate,
Silicon on Insulator,